ADVANCED FUZZY LOGIC CONTROL BASED DUAL-BUCK HALF-BRIDGE VOLTAGE BALANCER

S. V. V. S. K. Reddy[1] and Y. Srinivavasa Rao[2]

[1]Department of Electrical And Electronics Engineering Kakinada Institute Of Engineering And Technology-II Korangi, India.
[2]Department of Electrical And Electronics Engineering , Kakinada Institute Of Engineering And Technology Korangi,India.

Abstract:-The increasing demand for development of power from renewable energy has lead to creation of Micro-dc grid.In Micro-dc grid two wire transmission is widely acceptable but from the consideration of different voltage levels of power converters and loads this is unacceptable .In order to meet this a half bridge dual buck voltage balancer can be incorporated into micro dc-grid. This has the functionality to convert a two wire into three wire system via a neutral line. However peak shoot through problem in bridge converter will degrade the performance of voltage balancer .In this paper, a dual-buck voltage balancer and control strategy based on fuzzy logic control technique is proposed which can avoid peak shoot through problem. The controller design is presented and control parameters are evaluated based on inductor current, capacitors and unbalanced loads.Fuzzy logic controller is designed.Finally,the simulation results of proposed fuzzy control scheme are compared with the normal proportional control scheme.

Keywords: Dual-Buck,distributon system, half-bridge,micro-dc grid,voltage balancer,fuzzy logic control,two wire ,three wire system.

I.INTRODUCTION

A Distributed generation system Connected To D .C-Micro grid is capable of supplying high quality electric power is focused with the development of renewable energy source generation [2]-[8].The use of direct current allows simplifying the insertion between distribution.It needs only one interface converter with alternating current grid to make operation in islanding modeeasier,without compromising the safety of the public network[9] and it has definite benefit-a ine loss reduction[10].A micro-dc grid is also dependent on all types of converter ,such as bidirectional converter and dc converter[11],[12],grid-connected inverter[13],[15],voltage balancer[1]-[7].

However, a micro-dc grid has only one voltage level in two wire mode,and making it impossible to supply some loads at half voltage such as inverters needing a neutral line,converters with input voltage balancing like half-bridge converter and three-level bridge converter and so on. In particular, a micro-dc grid used in domestic and office places, a neutral connected to ground is favorable to security of the persons. Obviously, it is not possible with two wire mode to meet the requirements of all electronic devices. Thus a half-bridge was introduced to build a neutral line [1]-[7], which can easily convert a two wire dc grid to three-wire dc grid by a neutral line. In practice, the voltage balancer may be dispersedly used in any place where the voltage balance is needed, and of course, it can be placed at the output side of power supply center for building a whole three-wire dc grid. It is thus evident that voltage balancer improves the quality and flexibility of power supply in a micro-dc grid.

Unfortunately the topology of bridge-type converters suffer from shoot-through risk, which is a draw back to the reliability of this type of power converters .A dual-buck half-bridge converter can avoid the shoot-through problem, the free- wheeling diodes instead of body diodes of the switches, and all the switches and diodes operated at half of line cycle; thus efficiency is improved [16]-[21].

In this paper, a dual-buck half voltage balancer is proposed. For meeting the characteristic of the proposed voltage balancer, a control strategy of respectively driving the two bridge legs of proposed voltage balancer to work for high efficiency is also presented. In order to select the parameters of filter inductors and capacitors and to design the control system parameters ,the relationships of current of inductors, capacitors and unbalanced loads are described in detail. Fuzzy Logic Controller[10]-[14] is designed separately. Finally, simulation results are done and compared with Proportional controller and fuzzy controller for same voltage balancer.

II. TOPOLOGY AND CONTROL STRATEGY OF THE PROPOSED VOLTAGE BALANCER

A.Typical Structure of a Micro-DC Grid

A typical structure of a micro-dc grid [1]-[7] with a voltage balancer is shown in Fig. 1, where the voltage balancer is used to construct a neutral line achieving two same voltage levels for requirements of different types of loads, such as unbalanced loads, half-bridge converter and inverter, and so on

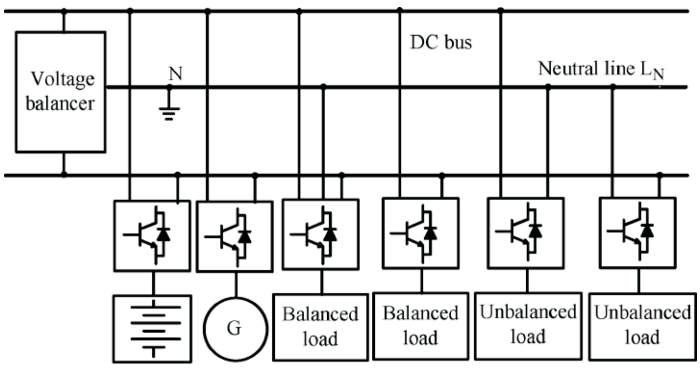


Fig 1.Typical structure of micro-dc grid.

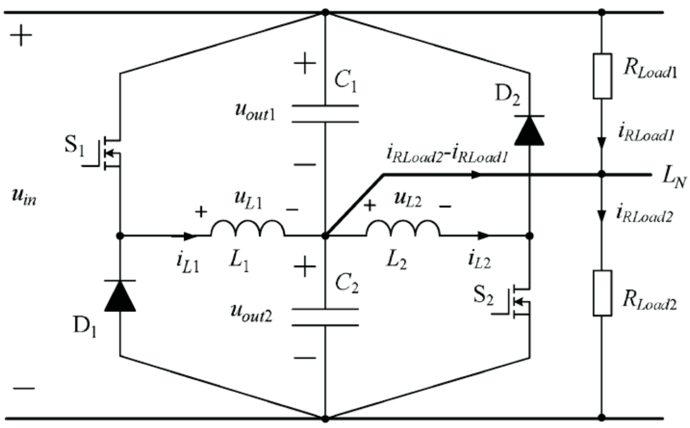


Fig 2.Proposed dual buck half-bridge voltage balancer

B.Proposed Voltage Balancer

The proposed voltage balancer- a dual buck half-bridge voltage is shown in Fig. 2, which is made up of a left bridge (S_1,D_1,L_1), a right bridge leg(S_2,D_2,L_2), and neutral line LN usually connected to earth ground. If the complementary driving technology is adopted between the switches S1 and S2, the two inductor currents i_{L1} and i_{L2}. Thus, the two inductor current will cause additional power losses. Obviously, the complementary operational technology does not use an advantage of the topology to improve the system efficiency. It is expected have a control strategy that can drive the left bridge leg and right bridge leg, respectively, based on different power quantity of unbalanced loads

C.Proposed Control Stratergy

The Proposed control strategy is presented in Fig. 3. The output signal u_e of voltage regulator is directly sent to control switch S_1, its negative value ($-u_e$) control the switch S_2. Combining Figs. 2 and 3, it may be concluded that, when R_{Load2} is lower than R_{Load1}, the signal u_e is positive and the left bridge leg will be driven while the right bridge leg will not work , and on the contrary, the signal ue is negative and the right bridge leg will be driven. It is thus clear that only one of the two bridge legs will work during every switching period and the loss of other bridge leg will be avoided compared with the complementary driving technology.

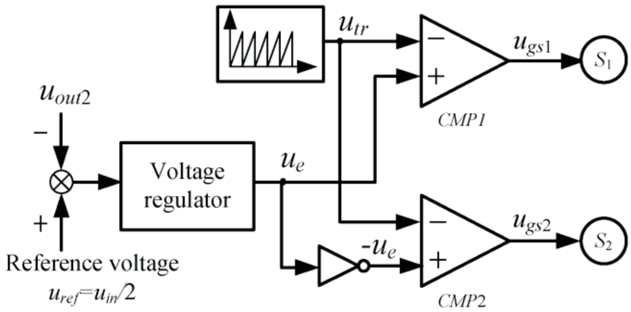


Fig. 3 Diagram of Proposed Control Strategy.

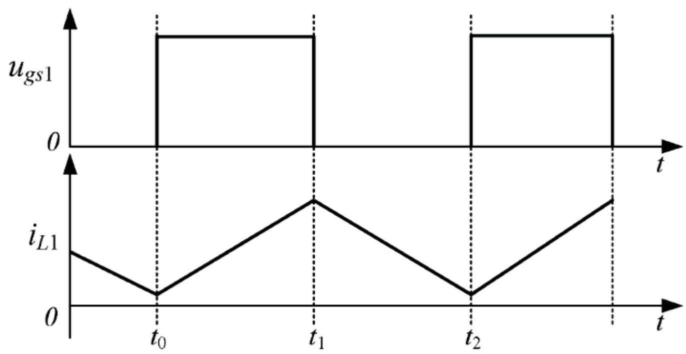


Fig. 4 Driving signal and inductor current waves under CCM.

III. OPERATING PRINCIPLE BASED ON THE PROPOSED CONTROL STRATEGY

As similar to buck converter, each bridge leg may be operates in continuous conduction mode(CCM) and discontinuous mode operation(DCM).For simplifying the analysis of the operational principle, some assumptions are made;1)All inductors and capacitors are ideal, $C_1=C_2=C$, and $L_1=L_2=L$; 2)the output voltage $u_{out1}=u_{out2}$ and are not changed during each switching process; and 3) all power switches and diodes are ideal devices with ignored switching time and conduction voltage drop. As the operating procedures of the right bridge leg are the same as those of the left bridge leg, only the analyzing principle of the left bridge leg is given.

A.CCM of Left Bridge Leg

The driving signal u_{gs1}, the current i_{L1}, and the equivalent circuits are shown in Figs 4 and 5, respectively, during CCM.

From Fig. 4, there are only two main operating modes during each switching period.

1) mode 1 [t_0,t_1] [Refer to Fig. 4 and 5(a)]:

The switch S1 is turned on at time t_0, and current iL1 increases linearly

$$L_1\frac{di_{L1}}{dt}=u_{in}-u_{out}=u_{out1} \quad (1)$$

During this mode, the input voltage uin sends additional energy to the load R_{Load2} through the inductor L_1.The voltage stress of the freewheeling diode D_1 is the input voltage u_{in}.

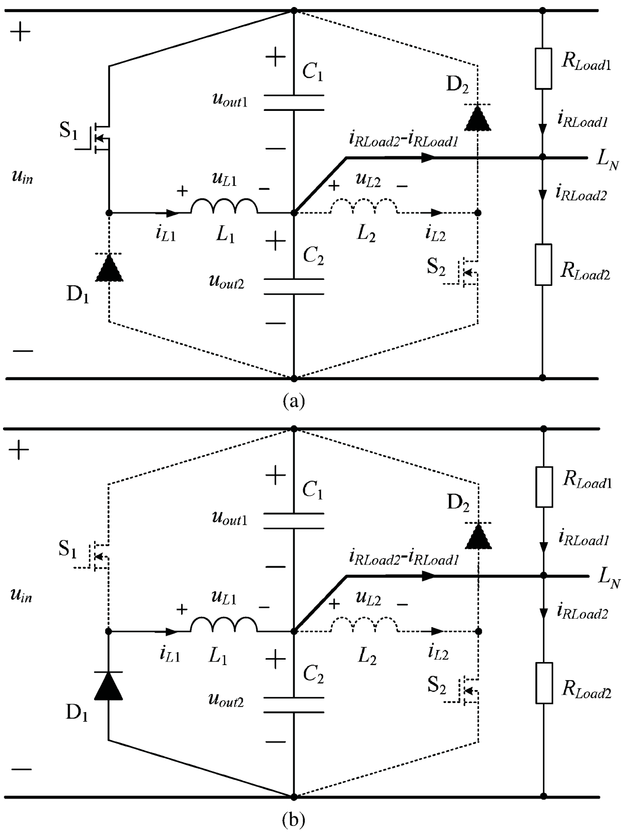


Fig. 5. Equivalent circuits under CCM (a)Mode 1. (b)Mode 2.

2) Mode 2[t_1,t_2] [Refer to Figs. 4 and 5(b)]:

The switch S_1 is turned off at the time t_1, and the current i_{L1} will continue to run through the freewheeling diode D_1. The current i_{L1} decreases linearly

$$L_1 \frac{di_{L1}}{dt} = -u_{out2} \qquad (2)$$

The procedure will end when the S_1 is turned on again the time t_2. During this mode, the voltage stress of the switch S_1 is also the input voltage uin. From the time t_2, a next operating period will start.

As the voltage uout1 is the same as u_{out2} under the stabilization and a voltage-second product of an inductor is zero during a period, it can be concluded

$$u_{out1}(t_1 - t_0) = u_{out}(t_2 - t_1) \qquad (3)$$

Thus, the time (t_1 — t_0) is equal to time (t_2 — t_1), i.e., the turn on time is equal to turn off time

B.DCM of Left bridge Leg:

There are three operating modes under DCM. The u_{gs1}, i_{L1}, and equal circuits are shown in Fig. 5-7, respectively. From Fig. 6, it can be concluded that the mode 1 [t_0,t_1] and the mode 2 [t_1,t_2] are in accordance with the two modes under CCM, respectively. Therefore, only the mode 3 [t_2,t_3] is given.

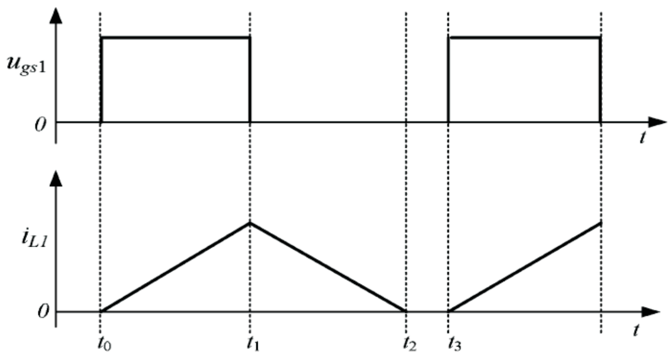


Fig.6. Driving signal and inductor current waves under DCM

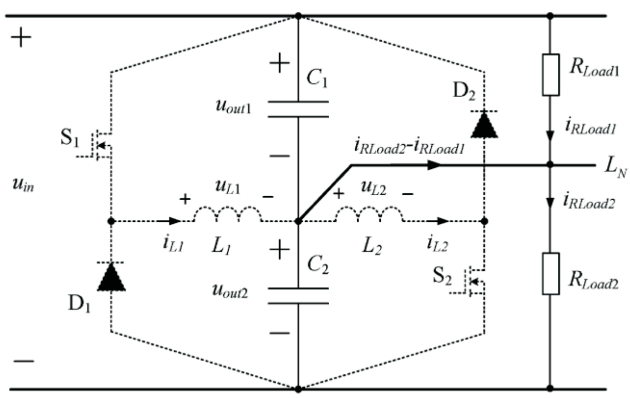


Fig .7 .Equivalent circuit of mode 3 under DCM

3) Mode 3 [t_2, t_3] [Refer to Figs. 6 and 7]:

From the time t_2, the loads R_{Load1} and R_{Load2} are supplied by the voltage source u_{out1} and u_{out2} because the current i_{L1} decreases to zero. According to the voltage-second product of an inductor, it is got from Fig. 6

$$u_{out1}(t_1 - t_0) = u_{out2}(t_2 - t_1) \quad (4)$$

IV. MAIN CURRENT RELATIONSHIPS

As is known to all, the current relationship of filter inductors and capacitors is the important basis for selecting the value of filter inductors and capacitors and building an average small signal model in power converters. Therefore, the main current relationships of the voltage balancer will be analyzed in detail. For simplifying the analysis, the current relationships are defined in Fig. 8, and waveforms are shown in Fig. 9. Because of having th e similar operating procedure, only the current relationships of left bridge leg operation is analyzed. The analysis of current relationships is divided into two parts according to value of inductor current i_{L1}.

A.Current i_{L1} Not Zero:

The current waveforms are shown in Fig. 9 during the time ($t_0 - t_2$). As the sum of u_{out1} and u_{out2} is equal to u_{in}, the ripple voltage Δu_{out1} of u_{out1} is also equal to the negative ripple voltage $-\Delta u_{out2}$ of u_{out2}

$$\Delta u_{out1} = \frac{1}{C_1}\int_{to}^{Ts} i_{C1}dt = \frac{1}{C_2}\int_{to}^{Ts} i_{C2}dt = -\Delta u_{out2} \quad (5)$$

Where $Ts = t_2 - t_0$ in Fig. 9(a) or $Ts = t_3 - t_0$ in Fig. 9(b).As the average value of the current i1 is the load currentiR_{Load1}, the ripple current $\Delta i1$ is equal to the current i_{C1} of the capacitor C_1. Thus, the ripple current Δi_2 is also equal to the current i_{C2} of the capacitor C_2

$$\begin{cases} \Delta i_1 = i_{C1} \\ \Delta i_2 = i_{C2} \end{cases} \quad (6)$$

According to (5) and (6), it yields under $C_1 = C_2$

$$\Delta i_1 = i_{C1} = -\Delta i_2 = -\Delta i_{C2} \quad (7)$$

As $i_2 = i1 + i_{L1}$, it can be got

$$\Delta i_{L1} = \Delta i_2 - \Delta i_1 \quad (8)$$

Where Δi_{L1} is the ripple current of the inductor L_1. It is obtained by using (7) and (8)

$$\Delta i_{L1} = 2i_{C2} = -2i_{C1} \quad (9)$$

Therefore, the Δi_{L1} is twice of the currents of i_{C1} and i_{C2}

B.Current iL1 Zero:

The current relationships are shown in Fig. 9(b) between the time t_2 and t_3. As i_{L1} is zero, the current i_1 and i_2 will not be associated with the current i_{L1}. That is to say, $i_1 = i_2$.

The powers P_{out1} and P_{out2} of the loads R_{Load1} and R_{Load2} are u^2_{out1}/R_{Load1} and u^2_{out2}/R_{Load2}, respectively. As the input power $P_{in}(P_{in} = u_{in} \times i_{in})$ is the sum of P_{out1} and P_{out2} without power losses, the current i_{in} is $(P_{out1} + P_{out2})/u_{in}$, which is equal to i_1 and i_2. Due to $u_{out1} = u_{out2}$ and $R_{Load2} < R_{Load1}$ under stable condition, we can get $i_2 < iR_{Load2}$ and $i_1 > iR_{Load1}$. Thus, the capacitor C_2 supplies a current ($i_{C2} = iR_{Load2} - i_2$) to the load R_{Load2} by discharging, which results in the u_{out2} linearly falling down, whereas the capacitor C_1 is charged by the current ($i_{C1} = i_1 - iR_{Load1}$), and the u_{out1} linearly rises. Because of $u_{out1} + u_{out2} = u_{in}$, the Δu_{out1} and i_{C1} are also equal to $-\Delta u_{out2}$ and $-i_{C2}$, respectively

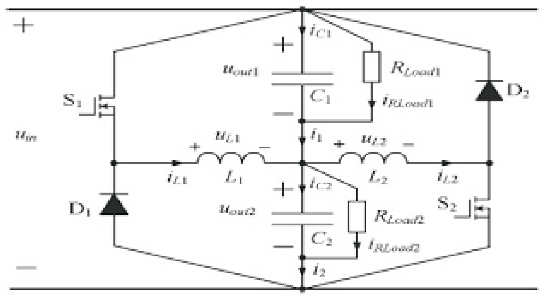


Fig. 8. Assigned diagram of the current relationships.

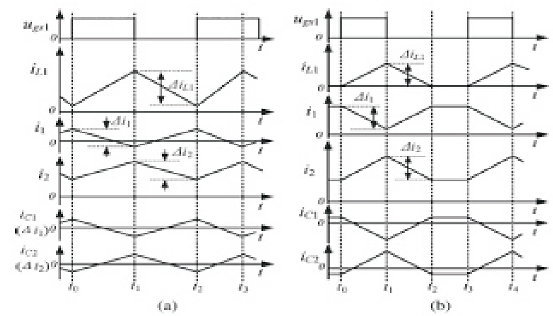


Fig. 9. Main current relationship waveforms of the left bridge leg. (a) CCM. (b) DCM.

V. . AVERAGE SMALL-SIGNAL MODEL

In order to select the control system parameters, the average small-signal model of the voltage balancer under CCM is derived. The duty cycles of S_1 and S_2 are defined as $d_1(d_1 = D_1 + \hat{d}_1)$ and $d_2(d_2 = D_2 + \hat{d}_2)$, respectively, where D_1, D_2, $\hat{d}_1$, and $\hat{d}_2$ are stable duty ratios and the perturbations of d_1 and d_2. Moreover, the voltage u_{in} and u_{out2} are defined as $u_{in} = U_{in} + \hat{u}_{in}$ and $u_{out2} = U_{out2} + \hat{u}_{out2}$, respectively, where U_{in}, U_{out2}, $\hat{u}_{in}$, and $\hat{u}_{out2}$ are the stable voltage values and the perturbations of u_{in} and u_{out2}.

A. Average Small-Signal Model of Left Bridge Leg:

From Fig. 8, we can obtain (10) and (11) when the left bridge leg operates under CCM.

1)S1 turning on

$$\begin{cases} u_{L1} = L_1 \dfrac{di_{L1}}{dt} = u_{in} - u_{out2} \\ i_{C2} = C_2 \dfrac{du_{out2}}{dt} = i_{L1} + C_1 \dfrac{d(u_{in} - u_{out2})}{dt} + \dfrac{u_{in} - u_{out2}}{R_{Load1}} - \dfrac{u_{out2}}{R_{Load2}} \end{cases} \tag{10}$$

2) S1 turning off

$$\begin{cases} u_{L1} = L_1 \dfrac{di_{L2}}{dt} = u_{in} - u_{out2} \\ i_{C2} = C_2 \dfrac{du_{out2}}{dt} = i_{L1} + C_1 \dfrac{d(u_{in} - u_{out2})}{dt} + \dfrac{u_{in} - u_{out2}}{R_{Load1}} - \dfrac{u_{out2}}{R_{Load2}} \end{cases} \tag{11}$$

According to the methods of building average model, it can be derived from (10) and (11)

$$\begin{cases} L\dfrac{d\hat{i}_{L1}}{dt} = -\hat{u}_{out2} - (D_1)\hat{u}_{in} + \hat{d}_1 U_{in} \\ 2C\dfrac{d\hat{u}_{out2}}{dt} = C\dfrac{d\hat{u}_{in}}{dt} + \dfrac{\hat{u}_{in}}{R_{Load1}} - (\dfrac{1}{R_{Load1}} + \dfrac{1}{R_{Load2}})\hat{u}_{out2} + \hat{i}_{L1} \end{cases} \tag{12}$$

Thus, the transfer function of the output voltage u_{out2} versus the duty cycle d_1 is presented by

$$G_{out2d}(s) = \frac{\hat{u}_{out2}(s)}{\hat{d}_1(s)} = \frac{Uin}{2LCS^2 + LS(\dfrac{1}{RLoad1} + \dfrac{1}{RLoad2}) + 1} \tag{13}$$

It is obvious that the transfer function is similar to that of a buck converter.

B. Average Small-Signal Model of Right Bridge Leg

1)S2 turning on

$$\begin{aligned} u_{L2} &= L_2 \frac{di_{L2}}{dt} = u_{in} - u_{out2} \\ i_{C2} &= C_2 \frac{du_{out2}}{dt} = C_1 \frac{d(u_{in} - u_{out2})}{dt} + \frac{u_{in} - u_{out2}}{R_{Load1}} - \frac{u_{out2}}{R_{Load2}} - i_{L2} \end{aligned} \tag{14}$$

2) S2 turning off

$$\begin{cases} L\dfrac{d\hat{i}_{L2}}{dt} = \hat{u}_{out2} - (1 - D_2)\hat{u}_{in} + \hat{d}_2 U_{in} \\ 2C\dfrac{d\hat{u}_{out2}}{dt} = C\dfrac{d\hat{u}_{in}}{dt} + \dfrac{\hat{u}_{in}}{R_{Load1}} - (\dfrac{1}{R_{Load1}} + \dfrac{1}{R_{Load2}})\hat{u}_{out2} - \hat{i}_{L2} \end{cases} \tag{15}$$

According to the methods of building average model, (14)and (15)are rewritten By

$$\begin{cases} L\dfrac{d\hat{i}_{L2}}{dt} = \hat{u}_{out2} - (1 - D_2)\hat{u}_{in} + \hat{d}_1 U_{in} \\ 2C\dfrac{d\hat{u}_{out2}}{dt} = C\dfrac{d\hat{u}_{in}}{dt} + \dfrac{\hat{u}_{in}}{R_{Load1}} - (\dfrac{1}{R_{Load1}} + \dfrac{1}{R_{Load2}})\hat{u}_{out2} - \hat{i}_{L2} \end{cases} \tag{16}$$

The transfer function of the output voltage u_{out2} versus the duty cycle d_2 is given by

$$G_{out2d2}(s) = \frac{\hat{u}_{out2}(s)}{\hat{d}_2(s)} = \frac{-U_{in}}{2LCS^2 + LS\left(\frac{1}{RLoad1} + \frac{1}{RLoad2}\right) + 1} \tag{17}$$

Comparing (13) and (17), the right bridge leg is running backward buck converter. Moreover, combining Fig. 3, equations (13), and (17), the control system diagram of the voltage balancer can be illustrated by Fig. 10, where K_m is the amplitude of the uni-polar triangle carrying wave u_{tr}, k is the feedback coefficient, and It is obvious that $G_{out2d}(S)$ is similar to the transfer function of a buck converter, and thus, the designing method of the control system parameters of the voltage balancer may be according to that of a buck converter.

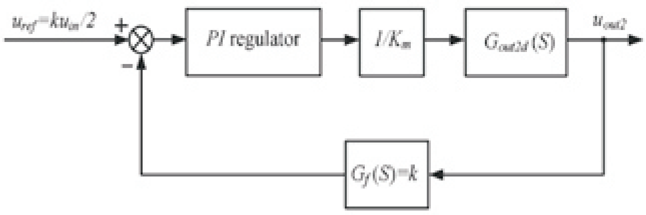


Fig. 10. Control system diagram.

VI. MODELING OF FUZZY CONTROLLER

Traditionally PD, PI and PID controller are most popular controllers and they are widely used in most power electronic

closed loop appliances, But in the recent year there are many researchers reported successfully adopted the Fuzzy Logic

Controller (FLC) to become one of intelligent controllers. Here we are using fuzzy logic controller with feedback of voltage output respectively. The voltage output in the circuit will be fed to fuzzy controller to give appropriate measure on steady state signal. Based on the human knowledge fuzzy logic control is built up by a group of rules of system behavior. For the dynamic behavior of dual buck converter and performance of proposed controllers we use Mat lab simulation. the design of fuzzy logic controller can provide desirable both large signal and small signal dynamic performance , which is not possible in linear control technique. Thus, fuzzy logic controller has an ability to improve the robustness of dual buck half bridge voltage balancer. The basic scheme of the controller consists of four principal components such as: a Fuzzification, which converts input data value into suitable linguistic values; a knowledge base, which consists of control rule set and a data base with the necessary linguistic definitions ; a Decision-Making logic ,which is use to simulating a human decision process and infer the fuzzy control action from the knowledge of the control rules and linguistic variable definitions; And a Defuzzification interface, which yields non fuzzy control action from an inferred fuzzy control action. An analysis of buck converter circuit revealed that the inductor current plays significant task in dynamic response of buck converter. it also provide the storage energy information in the converter. Thus, any changes in the inductor current may affect output voltage of the converter, output voltage will provide information of steady state condition of converter. However, the three main parameters need to be considered when designing buck converters are power switch, capacitor and inductor.

A.Fuzzy Logic Membership Function

The dual buck half bridge converter is a nonlinear function of the duty cycle because of the small signal model and its control method was applied to the control of buck converters. In Fuzzy controllers mathematical model is not require. Instead, they are designed based on general knowledge of the plant (converter). The Fuzzy controllers are designed to adopt the varying operating points. Fuzzy Logic Controller is designed to control the output of buck dc-dc converter. In the fuzzy logic system two input variables, error (e) and change of error (de) and one output variable (u) is duty cycle of PWM output are used. For each input and output variable fuzzy sets must be defined. As shown in Fig. 2. The five fuzzy subsets PS (Positive Small), PB (Positive Big), ZE (Zero), NS (Negative Small), NB (Negative Big) has been chosen for input variables error (e) and change of error (de). The Triangular shape has been adopted for the membership functions; the value of each input and output variable is normalized in the range[-1,1] by using suitable scale factors.

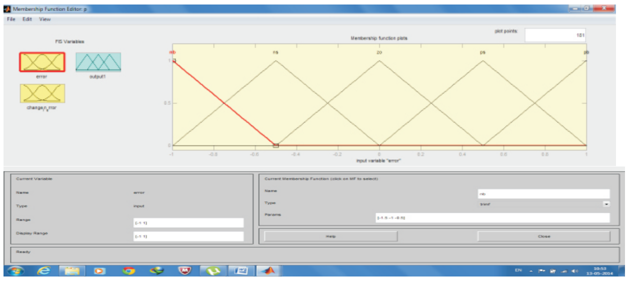


Fig. 11. The Membership Function plots of error

Fig. 12 The Membership Function plots of change error

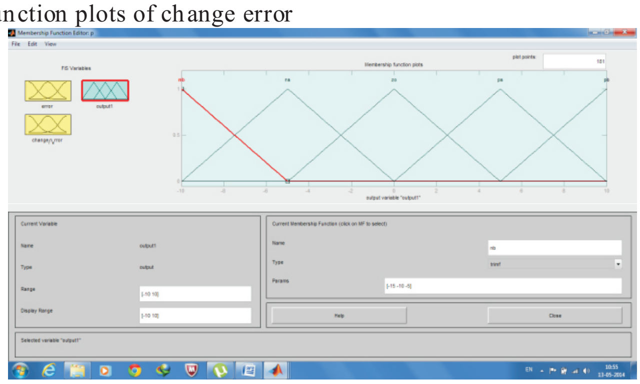


Fig. 13 The Membership Function plots of change error

B. Fuzzy Logic Table Rules

Fuzzy controller rules which are play a very important role for controller simulation are obtained from the analysis of the system behavior. In their formulation it must be considered that, By using this controller we improve the converter performances in terms of dynamic response and robustness. when the output voltage is far from the set point i.e error (e) is NB or PB, the controller must be do the strong corrective action i.e duty cycle close to zero or have the dynamic response as fast as possible, obviously taking into account current limit specifications of the system.

Table 1: Rules for error and change of error

(e) / (de)	NB	NS	ZO	PS	PB
NB	NB	NB	NB	NS	ZO
NS	NB	NB	NS	ZO	PS
ZO	NB	NS	ZO	PS	PB
PS	NS	ZO	PS	PB	PB
PB	ZO	PS	PB	PB	PB

Second, when output voltage error of the system approaches to zero i.e error (e) is ZE, NS, PS then in order to ensure stability around the working point, the current error should be properly taken into account. when the current value approaches the limit value, suitable rules must be introduced to preventing the large overshoots. The rules of fuzzy control for error and change of error can be referred in the table 1:

VII. SIMULATION RESULTS

In order to confirm the aforementioned analysis, the computer simulations of the main current relationships and the loads transiently changing are carried out with proportional controller and fuzzy controller separately by using software mat lab/simulink, and the other condition simulations are ignored. Considering single phase 110 V for a half-bridge inverter and single phase 220 V for a full-bridge inverter, the dc bus voltage (input voltage uin) is selected to be 360 V. The other main simulation parameters are listed: switching frequency of 25 kHz, $L_1 = L_2 = 230$ µH, and $C_1 = C_2 = 470$ µF.

A. Simulations of the Current Relationships

In this section, the simulation results of the current relationships in both D.C.M and C.C.M mode are given for fuzzy controller and proportional controller. The simulation results of the current relationships are given in Fig. 14. In Fig. 14, it includes CCM [R_{Load1} = 100 O and R_{Load2} =10 O as shown in Fig. 14 ,17] and DCM [R_{Load1} = 40 O and R_{Load2} = 30 O as shown in Fig. 15,18]. As seen from Fig. 14, under nonzero i_{L1}, it can be easily concluded that $\Delta u_{out1} = -\Delta u_{out2}$, $i_{C1} = i_{C2}$, and $\Delta i_{L1} = i_{C2} - i_{C1}$.

When the inductor current i_{L1} is zero, we can get $P_{out1} = u^2_{out1}/R_{Load1}$ = 810 W, $P_{out2} = u^2_{out2}/R_{Load2}$ =1080 W, $i_{in} = (P_{out1} + P_{out2})/u_{in}$ = 5.25 A, $i_2 = i_1 = i_{in}$ =5.25 A, $i_{RLoad1} = u_{out1}/R_{Load1}$ = 4.5 A, and $i_{RLoad2} = u_{out2}/R_{Load2}$ = 6 A under steady state. Because of $i_2 < i_{RLoad2}$, the lacking current ($i_2 - i_{RLoad2}$ = - 0.75 A = i_{C2})is supplied by the capacitor C_2 discharging, and the voltage u_{out2} linearly drops. Due to $i_1 > i_{RLoad1}$, the capacitor C_1 is charged by the surplus nearly rises. These states are presented in Fig. 15.

B. Simulations of Loads Changing

Fig. 16,19 shows the simulation results of loads transiently changing with fuzzy controller and proportional controller , where Fig. 16(a),19(a) gives the results of the load current i_{RLoad2} = 2.3 A and the load current i_{RLoad1} changes from 0 to 6.7 A; Fig. 16(b),19(b) describes the results of i_{RLoad1} = 1.8 A, and the i_{RLoad2} changes from 0 to 5 A.As seen from Fig. 16,19 the left bridge leg will operate wheniR$_{Load2}$ is larger than i_{RLoad1}; otherwise, the right bridge leg will run. At the same time, the output voltages u_{out1} and u_{out2} are nearly equal, although they have obvious fluctuations when the loads are instantly changed. The fluctuations are mainly caused by a longer regulated time of the voltage regulator whose output signal polarity is altered under transiently changing loads as seen from Fig.3.

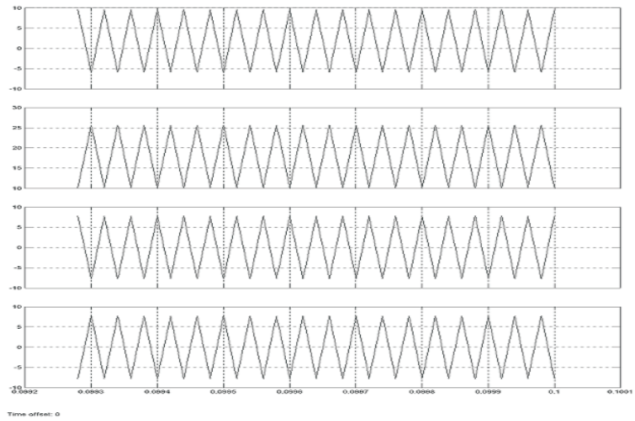


Fig.14 Simulation results of current relationships in C.C.M mode with proportional controller

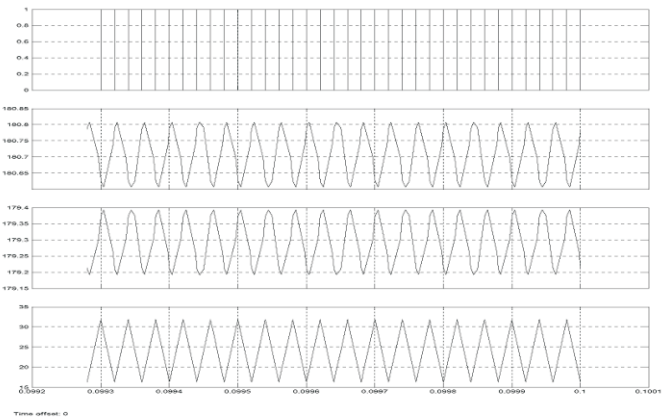
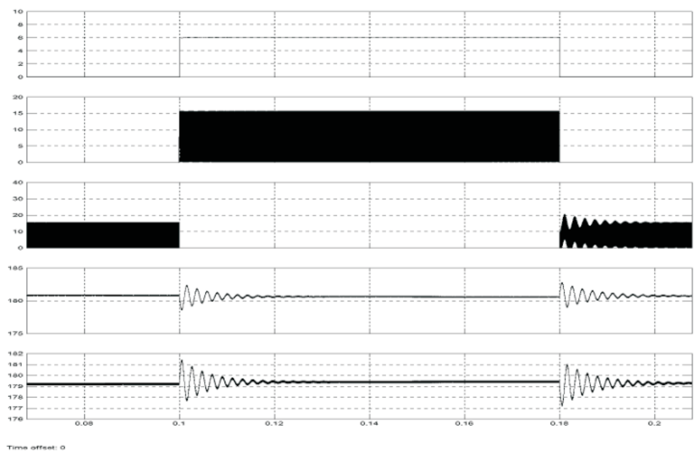
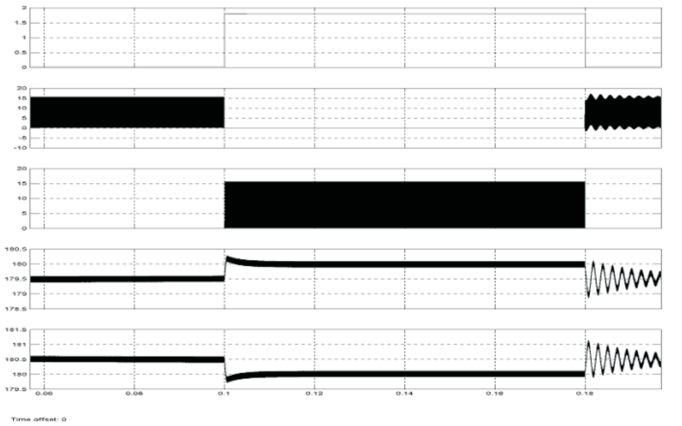


Fig.15 Simulation results of current relationships in D.C.M mode with proportional controller



(a)



(b)

Fig.16 Simulation results under loads transiently changing (a)R_{Load1} changing (b) R_{load2} changing with proportional controller

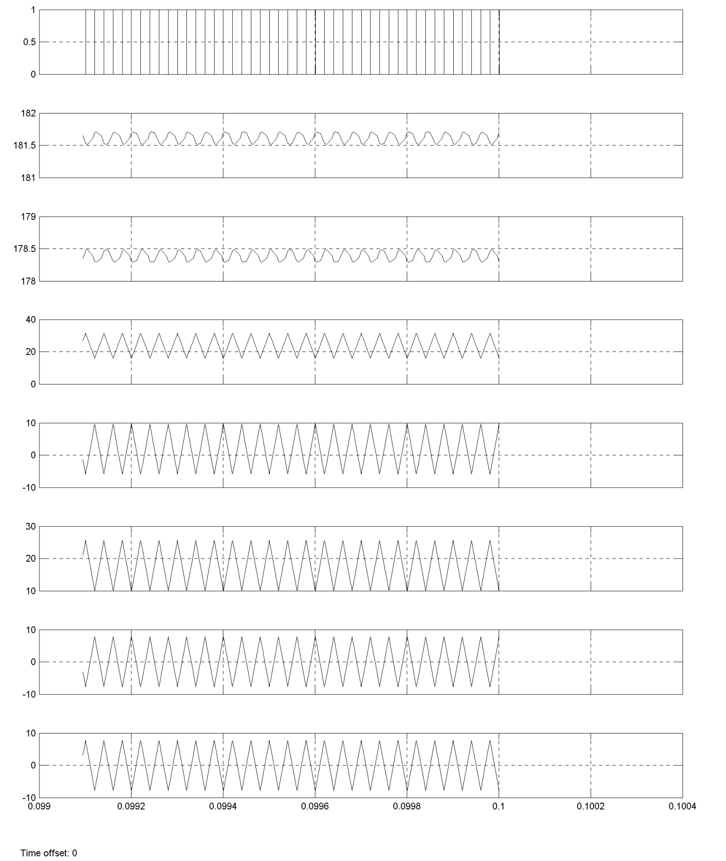


Fig.17. Simulation results of current relationships in C.C.M mode with fuzzy controller

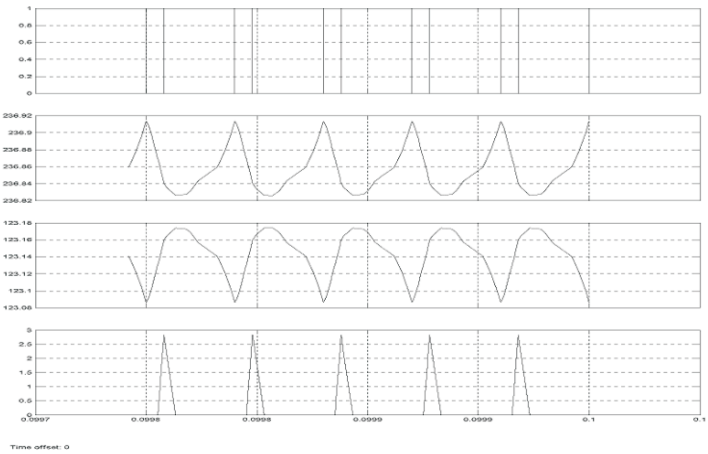
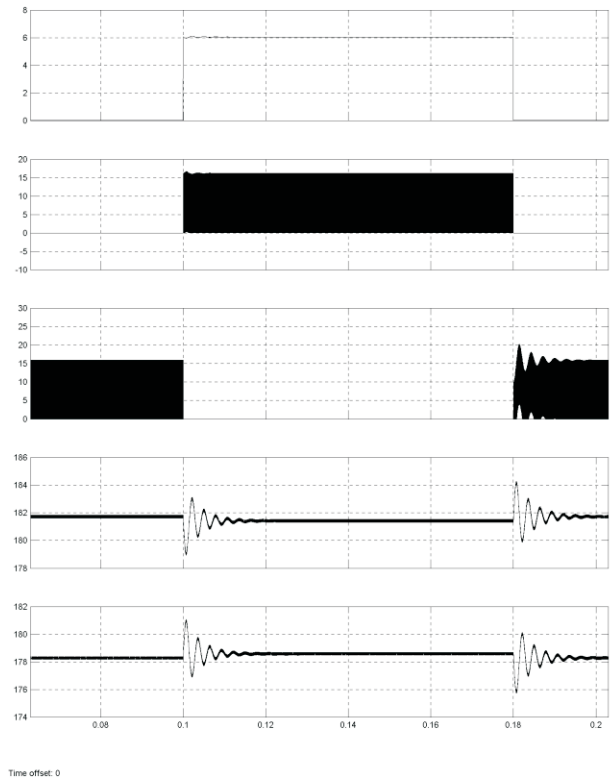
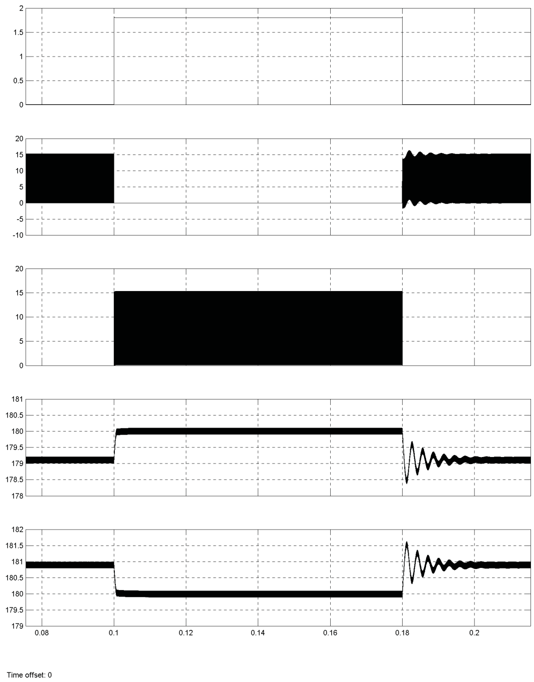


Fig.18. Simulation results of current relationships in D.C.M mode with fuzzy controller



(a)



(b)

Fig.19 Simulation results under loads transiently changing (a)R_{Load1}changing (b) R_{load2} changing with Fuzzy controller.

C.Comparitive Analysis

Using Simulation ,the performance of Half bridge dual buck voltage balancer using both the controllers are compared. The comparison parameters used are

(i)Settling time(t_s)in secs
(ii) Peak overshoot(M_p) in volt
(iii) Integrated square error
(iv) Steady state error

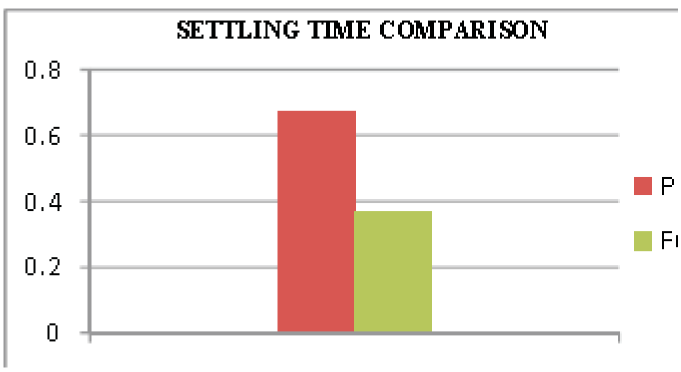


Fig. 20:Settling time comparison between P and Fuzzy

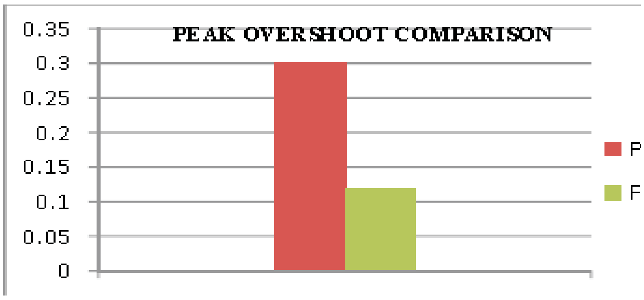


Fig.21:Peak overshoot comparison between P and Fuzzy

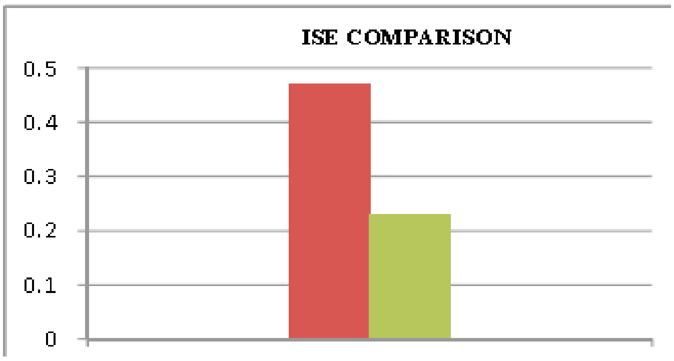


Fig.22:Integrated Square Error comparison between P and Fuzzy

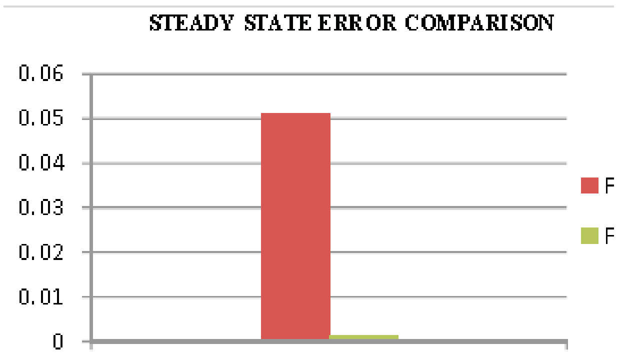


Fig.23:Steady state Error comparison between P and Fuzzy From the simulation results the following conclusion can be obtained.

1.Fuzzy controller requires very low settling time for output voltages compared to P controller.
2.Fuzzy controller causes low peak overshoot in output voltages compared to P controller.
3.The Integrated square error of output voltages is reduced using fuzzy controllers compared to P controller.
4. The Steady state error of output voltages is also reduced using fuzzy controllers compared to P controller.

VIII. CONCLUSION

In this paper, a dual-buck half-bridge voltage balancer and its control strategy are proposed. This type of voltage balancer can well resolve the shoot-through problem. It can build a neutral line to balance two output voltage for different loads .The simulation results of same control strategy with proportional and fuzzy controller are done. Finally, the fuzzy controller based half bridge dual buck voltage balancer has good ability of balancing output voltage even under different input voltage and less shoot-through compared to P- controller

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S. V. V. S. K. Reddy
Department of Electrical And Electronics Engineering Kakinada Institute Of Engineering And Technology-II Korangi, India.

Y. Srinivavasa Rao
Department of Electrical And Electronics Engineering , Kakinada Institute Of Engineering And Technology Korangi,India.